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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/032,876	10/24/2001	Kamel Ayadi	13292-003001	7126

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EXAMINER
TSAI, CAROL S W

ART UNIT	PAPER NUMBER
2857	

DATE MAILED: 06/25/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Applicati n No.	Applicant(s)	
	10/032,876	AYADI, KAMEL	
	Examiner	Art Unit	
	Carol S Tsai	2857	

-- Th MAILING DATE of this communication appears n th cover sheet with the correspondence address --

Period f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 October 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disp sition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 February 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description:

"28" in page 8, lines 8.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 2, 9-11, 18-20, and 25-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over U. S. Patent No. 5,206,582 to Ekstedt et al. in view of U. S. Patent No. 6,484,116 to Yokoyama.

With respect to claims 1, 2, 9, 18, and 25, Ekstedt et al. disclose a system, comprising: an input/output device (I/O device 18 shown on Fig. 1) of a computer system (controller 16 shown on Fig. 1); one or more test instruments (measurement instruments 10 shown on Fig.1) producing a set of electrical signals; a probe card (probe card 14 shown on Fig. 1) having a plurality of

probe needles used for measuring electronic characteristics of each of a plurality of devices on a semiconductor wafer, each device having a plurality of cells, each cell having a set of bond pads; a matrix switch (relay matrix 12 shown on Fig. 1); and an interface conduit electrically connecting the one or more test instruments, the computer, the probe card, and the matrix switch together, the semiconductor wafer moving so that the probe needles measure the electrical characteristics of each cell for each device selected for testing (see Figs. 1 and 8; col. 3, line 42 to col. 4, line 6; and col. 10, line 15 to col. 12, line 5).

Ekstedt et al. do not disclose a graphical user interface.

Yokoyama teaches a graphical user interface (GUI processing section 26 shown on Fig. 2).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Ekstedt et al.'s system to include a graphical user interface, as taught by Yokoyama, in order to allow input/output of various data with the user through a GUI function in operations of the sequence setting section, the function setting section and the debugging execution section other than the parameter calculation section (see Yokoyama col. 5, lines 16-20).

As to claims 10, 19, and 26, Ekstedt et al. also disclose sending a signal to activate a plurality of test instruments (see col. 11, lines 4-20).

As to claims 11, 20, and 27, Ekstedt et al. do not disclose expressly determining if the plurality of test instruments being electrically connected.

It is, however, considered inherent that Ekstedt et al. determine if the plurality of test instruments being electrically connected (see col. 10, lines 32-51), because such determination is known to be necessary in order that testing can be successfully performed without failure.

4. Claims 3-6, 12-15, 21, 22, and 28-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ekstedt et al. in view of Yokoyama as applied to claims 1, 2, 9-11, 18-20, and 25-27 above, and further in view of U. S. Patent No. 6,223,098 to Cheong et al.

As noted above, with respect to claims 3, 12, 21, and 28, Ekstedt et al. in combination with Yokoyama teach all the features of the claimed invention, but do not disclose the user selecting either an automatic test mode or a manual test mode of the semiconductor wafer.

Cheong et al. teach the user selecting either an automatic test mode or a manual test mode of the semiconductor wafer (see col. 4, lines 41-45).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Ekstedt et al. in combination with Yokoyama's system to include the user selecting either an automatic test mode or a manual test mode of the semiconductor wafer, as taught by Cheong et al., in order to that operator can have option to select either a automatic test or manual test.

As to claim 4, Ekstedt et al. do not disclose the user setting the electrical signals of the test instruments through the GUI.

Yokoyama teaches the user setting the electrical signals of the test instruments through the GUI (see Figs. 1 and 2 and col. 3, line 62 to col. 4, line 56).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Ekstedt et al.'s system to include the user setting the electrical signals of the test instruments through the GUI, as taught by Yokoyama, in order to allow input/output of various data with the user through a GUI function in operations of the sequence setting section, the function setting section and the debugging execution section other than the parameter calculation section (see Yokoyama col. 5, lines 16-20).

As to claim 5, Ekstedt et al. also disclose the probe card transmitting a set of electrical signals from each test instrument through the probe needles to each set of bond pads and generating a test result for each device that is displayed graphically on the display (see col. 3, line 42 to col. 4, line 6).

As to claims 6, 15, and 30, Ekstedt et al. also disclose a pulse generator and a parametric analyzer (see col. 3, lines 42-48).

As to claims 13, 14, 22, and 29, Ekstedt et al. also disclose generating an output file for all devices tested and graphing data in the output file on a display (see col. 4, lines 2-6 and lines 57-58).

5. Claims 7, 16, 23, and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ekstedt et al. in view of Yokoyama as applied to claims 1, 9, 18, and 25 above, and further in view of U. S. Patent No. 5,986,281 to Burchanowski et al.

As noted above, with respect to claims 7, 16, 23, and 31, Ekstedt et al. in combination with Yokoyama teach all the features of the claimed invention, but do not disclose measuring a silicon band gap voltage.

Burchanowski et al. teach measuring a silicon band gap voltage (see col. 5, lines 16-25).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Ekstedt et al. in combination with Yokoyama's system to include measuring a silicon band gap voltage, as taught by Burchanowski et al., in order that reliable indication of the presence or absence of mobile ions can be obtained (see Burchanowski et al. Abstract, lines 9-10).

6. Claims 8, 17, 24, and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ekstedt et al. in view of Yokoyama as applied to claims 1, 9, 18, and 25 above, and further in view of U. S. Publication 2002/0152046 to Velichko et al.

As noted above, with respect to claims 8, 17, 24, and 32, Ekstedt et al. in combination with Yokoyama teach all the features of the claimed invention, but do not disclose measuring a capacitance.

Velichko et al. teach measuring a capacitance (see paragraphs 0003 and 0029).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Ekstedt et al. in view of Yokoyama's system to include measuring a capacitance, as taught by Velichko et al., in order to ensure that a fabricated structure on the semiconductor meets the specifications and requirements of the semiconductor manufacturer and falls within acceptable tolerances (see Velichko et al. paragraph 0003, lines 7-10).

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Gefen discloses systems and methods relating to semiconductor testing and programming, including semiconductor-chip testing apparatuses, semiconductor-chip programming apparatuses, semiconductor testing integrated-circuit chips ("TIC's"), employable in testing and/or programming semiconductor integrated circuits.

Nuxoll et al. disclose semiconductor devices having terminal arrangements in which mirrored pairs of the semiconductor devices can be tested by a common test device.

Allard, JR. et al. disclose a method and apparatus for automated testing of a plurality of electrostatic discharge (ESD) devices on a wafer.

Sato discloses a testing apparatus designed for testing semiconductor elements formed on a semiconductor wafer.

Holden discloses a probe card design method which optimizes the number of die probed per touchdown and minimizes the number of steps required to test an integrated circuit wafer.

Thatcher et al. disclose a method and apparatus for testing integrated circuit interconnect and measuring the value of passive component interconnecting the IC's.

Chen et al. disclose watchdog system having data differentiating means for use in monitoring of semiconductor wafer testing line.

Contact Information

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Carol S. Tsai whose telephone number is (703) 305-0851. The examiner can normally be reached on Monday-Friday from 7:30 AM to 4:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S. Hoff can be reached on (703) 308-1677. The fax number for TC 2800 is (703) 308-7382. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the TC 2800 receptionist whose telephone number is (703) 308-1782.

In order to reduce pendency and avoid potential delays, Group 2800 is encouraging FAXing of responses to Office actions directly into the Group at (703) 308-7382. This practice may be used for filing papers not requiring a fee. It may also be used for filing papers which require a fee by applicants who authorize charges to a PTO deposit account. Please identify the examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2800 will be promptly forwarded to the examiner.

Carol S. Tsai

06/17/03

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